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Note : Remove “Table of Content” before including in CP Book

18ECL38 : DIGITAL ELECTRONICS LABORATORY

A. LABORATORY INFORMATION

1. Lab Overview

Degree:	BE	*Program:*	EC
Year / Semester :	2/ 3	*Academic Year:*	2019-20
CourseTitle:	DIGITAL SYSTEM DESIGN LABORATORY	*Course Code:*	18ECL38
Credit / L-T-P:	2 / 1-0-1	*SEE Duration:*	180 Minutes
Total Contact Hours:	36 Hrs	*SEE Marks:*	60Marks
CIA Marks:	40	*Assignment*	1 / Module
Course Plan Author:	Mrs Kiranmayi M	*Sign*	Dt :
Checked By:		*Sign*	Dt :

2. Lab Content

Unit	Title of the Experiments	Lab Hours	Concept	Blooms Level
1	De-Morgan's law &Boolean expression relization using logic gates	03	Demorgan's Theorem	L3 Understand
2	FullAdderandSubtractor	03	Adder &Subtractor	L4 Analyze
3	Parallel Adder/Subtractor using 7483	03	Parallel Adder/Subtractor	L5 Evaluate
4	Comparators	03	Comparators	L5
5	Multiplexer	03	MUX	L4
6	Demultiplexerand Decoder	03	DEMUXand Decoder	L4
7	Study of Flip-Flops	03	Flip-Flopverification	L3
8	ShiftRegisters	03	ShiftRegisters	L3
9	RingCounter andJohnsonCounter	03	Ring/JohnsonCounter	L3

10	Synchronous Counters	03	Counters	L3
11	Simulate Serial Adder using simulation tool.	03	Serial- Adder simulation	L4
12	Simulate Binary Multiplier using simulation tool	03	Binary Multiplier	L4

3. Lab Material

Unit	Details	Available
1	Text books	
	1. Digital Logic Applications and Design, John M Yarbrough, Thomson Learning, 2001. ISBN 981-240-062-1.	In Lib
	2. Donald D. Givone, "Digital Principles and Design", Mc Graw Hill, 2002. ISBN 978-0-07-052906-9.	
2	Reference books	
	1. D. P. Kothari and J. S Dhillon, "Digital Circuits and Design", Pearson, 2016, ISBN:9789332543539.	In dept
	2. Morris Mano, —Digital design, Prentice Hall of India, Third Edition.	
	3. Charles H Roth, Jr., "Fundamentals of logic design", Cengage Learning.	
	4. K. A. Navas, "Electronics Lab Manual", Volume I, PHI, 5 th Edition, 2015, ISBN: 9788120351424.	
3	Others (Web, Video, Simulation, Notes etc.)	
		Not Available

4. Lab Prerequisites:

-	-	Base Course:		-	-
SNo	Course Code	Course Name	Topic / Description	Sem	Remarks
1	18ELN14	Basic Electronics	Knowledge on Digital electronics, boolean laws, basic gates	2	

			Knowledge of Filp-flops	-	Plan Gap Course

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

5. General Instructions

SNo	Instructions	Remarks
1	Observation book and Lab record are compulsory.	
2	Students should report to the concerned lab as per the time table.	
3	After completion of the Experiment, certification/signof the concerned staff in-charge in the observation book is necessary.	
4	Student should bring a notebook of 100 pages and should enter the readings /observations into the notebook while performing the experiment.	
5	The record of observations along with the detailed experimental procedure of the experiment in the Immediate last session should be submitted and certified/signed bystaff member in-charge.	
6	Should attempt all Experiments/ assignments given in the experimentlist session wise.	
7	When the experiment is completed, should disconnect the setup made by them, and should return all the components/instruments taken for the purpose.	
8	Any damage of the equipment or burn-out components will be viewed seriously either by putting penalty or by dismissing the total group of students from the lab for the semester/year	
9	Completed lab assignments should be submitted in the form of a Lab Record in which you have to write the logic diagrams, Truth table, expressions, simplification stepsand output for various inputs given	

6. Lab Specific Instructions

SNo	Specific Instructions	Remarks
1	Start writing the logic diagrams with the pin numbers	
2	Estimate the components required to perform the experiment (No. of	

	IC's, Pathcards)	
3	Use the trainer kit &Make the connections as per Logic diagram	
4	Turn on the power supply and check for the output	
5	Check for the Errors in connection and correct it	
6	Notedown the inputand output valuesand compare with original truth table	
7	Perform the Experiment for different inputs	

B. OBE PARAMETERS

1. Lab / Course Outcomes

#	COs	Teach. Hours	Concept	Instr Method	Assessment Method	Blooms' Level
1	Verify &understand De-Morgan's theorem &realize the boolean expression using logic gates	03	Demorgan's Theorem	Demonstrate	Oral questions	L3 Understand
2	Analyze the full adder/subtractor logic using logic gates	03	Full Adder &Subtractor	Demonstrate	Oral question and realization	L4 Analyze
3	Design the parallel adder &subtractor circuits and compare both the circuits	03	Parallel Adder/Subtractor	Demonstrate	Assignment and Slip Test	L5 Evaluate
4	Evaluate the performance of 4-bit magnitude comparator using 7485 IC	03	Comparators	Tutorial	Assignment	L5
5	Realize 4:1 mux &8:1 mux and Analyze the both	03	MUX	Demonstrate		L4
6	Realize 1:8 Demux &3:8 Decoder using 74138 IC	03	DEMUXand Decoder	Tutorial	Assignment	L4
7	Realize the operation of clocked SR &JK flip-flop.	03	Flip-Flopverification	Demonstrate	Assignment and Slip Test	L3
8	Understand the operation of shift registers	03	ShiftRegisters	lecture	Assignment	L3
9	differentiate Ring counter &Johnson	03	Ring/Johns	Demons	Assignment	L3

	counter using 7476 IC		onCounter	trate		
10	Realize the 3 bit counters and verify with truth table	03	Counters	Demonstrate	Oral questions	L3
11	Analyze the Serial adder simulation process	03	Serial simulation	Simulation	Assignment	L4
12	Simulate the working of a Binary Multiplier	03	Binary Multiplier	Simulation	Assignment	L4
-	**Total**	**36**	-	-	-	-

Note: Identify a max of 2 Concepts per unit. Write 1 CO per concept.

2. Lab Applications

SNo	Application Area	CO	Level
1	Engineering – Building circuits,Set Theory – Venn diagrams, Java	CO1	L3 Understand
2	integrated in the calculators and At Networking side the Full adder is used mostly.	CO2	L4 Analyze
3	CPLD applications and VHDL circuits and devices	CO3	L5 Evaluate
4	Generally, in electronics, the comparatoris used to compare two voltages or currents	CO4	L5
5	Communication System for the process of data transmission.	CO5	L4
6	Communication System which converts multiplexed signals back to the original form/ wireless or wired media	CO6	L4
7	main components of sequential circuitsm, storing of binary data, counter, transferring binary data from one location to other	CO7	L3
8	Temporary data storage, Data transfer, Data manipulation And incounters.	CO8	L3
9	count the data in a continuous loop, used in frequency divider circuits, 3 phase square wave generator , BCD counter etc	CO9	L3
10	Alarm clock, Set an AC timer, Set a timer for taking picture, finite state machines etc	CO10	L3

11	Engineering – Building circuits,Set Theory – Venn diagrams	CO11	L4
12	dividers for clock signals,finite state machines etc	CO12	L4

Note: Write 1 or 2 applications per CO.

3. Articulation Matrix

(CO – PO MAPPING)

-	Course Outcomes	Program Outcomes												
#	COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	Level
18ECL38.1	Verify & understand De-Morgan's theorem &realize the boolean expression using logic gates	3	2	2										L3
18ECL38.2	Analyze the full adder/subtractor logic using logic gates	3	2	2										L3
18ECL38.3	Design the parallel adder &subtractor circuits and compare both the circuits	3	2	2										L3
18ECL38.4	Evaluate the performance of 4-bit magnitude comparator using 7485 IC	3	2	2										L3
18ECL38.5	Realize 4:1 mux &8:1 mux and Analyze the both	3	2	2										L3
18ECL38.6	Realize 1:8 Demux &3:8 Decoder using 74138 IC	3	2	2										L3
18ECL38.7	Realize the operation of clocked SR &JK flip-flop.	3	2	2										L3
18ECL38.8	Understand the operation of shift registers	3	2	2										L3
18ECL38.9	differentiate Ring counter &Johnson counter using 7476 IC	3	2	2										L3
18ECL38.10	Realize the 3 bit counters and verify with truth table	3	2	2										L3
18ECL38.11	Analyze the Serial adder simulation process	3	2	2		2								L3
18ECL38.12	Simulate the working of Binary Multiplier	3	2	2		2								L3
18ECL38	Average	3	2	2		2								

Note: Mention the mapping strength as 1, 2, or 3

4. Mapping Justification

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Mapping		Mapping Level	Justification
CO	**PO**	-	-
CO1	PO1	L1	Basic knowledge of mathematics is essential to understand the combinatorial circuit design to build complex system like processor.
CO1	PO2	L2	Simple mathematical analysis is required to build complex system like micro-controllers using combinatorial logic.
CO1	PO3	L2	Strong foundation in designing and modeling of combinatorial logic circuits enables to provide design solutions for complex engineering problems like Arithmetic and logic units.
CO2	PO1	L1	Basic knowledge of mathematics is essential to design adder and subtractors which are used in building complex system like Digital signal processors and ASIC's.
CO2	PO2	L2	Simple mathematical analysis is required to build complex system like DSP Processors using basic adder and subtractors.
CO2	PO3	L2	Strong foundation in designing adder and subtractor circuits enables to provide design solutions for complex engineering problems like ASIC's and high speed processors.
CO3	PO1	L1	Basic knowledge of mathematics is essential to design adder and subtractors which are used in building complex system like Digital signal processors and ASIC's.
CO3	PO2	L2	Simple mathematical analysis is required to build complex system like DSP Processors using basic adder and subtractors.
CO3	PO3	L2	Strong foundation in designing adder and subtractor circuits enables to provide design solutions for complex engineering problems like ASIC's and high speed processors.
CO4	PO1	L1	Basic knowledge of mathematics is essential to design comparator which are used in building complex system like Digital signal processors and ASIC's.
CO4	PO2	L2	Simple mathematical analysis is required to build complex system like DSP Processors using basic comparators.
CO4	PO3	L2	Strong foundation in designing comparator circuits enables to provide design solutions for complex engineering problems like ASIC's and high speed processors.

CO5	PO1	L1	Basic knowledge of mathematics is essential to design multiplexers which are used in building complex system like processor.
CO5	PO2	L2	Simple mathematical analysis is required to build complex system like micro-controllers using combinational circuits like multiplexers
CO5	PO3	L2	Strong foundation in designing combinational circuits enables to provide design solutions for complex engineering problems like Arithmetic and logic units.
CO6	PO1	L1	Basic knowledge of mathematics is essential to design decoders and de-multiplexers which are used in building complex system like processor.
CO6	PO2	L2	Simple mathematical analysis is required to build complex system like micro-controllers using combinational circuits like decoders and de-multiplexers.
CO6	PO3	L2	Strong foundation in designing combinational circuits enables to provide design solutions for complex engineering problems like Arithmetic and logic units.
CO`7	PO1	L1	Basic knowledge of mathematics is essential to design flip-flop which are used in building complex system like memories.
CO7	PO2	L2	Simple mathematical analysis is required to build complex system like micro-controllers using basic flip flops.
CO7	PO3	L2	Strong foundation in designing flip-flop circuits enables to provide design solutions for complex engineering problems like memories.
CO8	PO1	L1	Basic knowledge of mathematics is essential to design shift registers which are used in building complex system like memories.
CO8	PO2	L2	Simple mathematical analysis is required to build complex system like micro-controllers using basic shift registers.
CO8	PO3	L2	Strong foundation in designing shift registers circuits enables to provide design solutions for complex engineering problems like memories.
CO9	PO1	L1	Basic knowledge of mathematics is essential to design counters which are used in building complex system in medical field like ECG counter.
CO9	PO2	L2	Simple mathematical analysis is required to build complex system like micro-controllers, timers using basic counters.

CO9	PO3	L2	Strong foundation in designing counter circuits enables to provide design solutions for complex engineering problems like timers and counters in processors and controllers.
CO10	PO1	L1	Basic knowledge of mathematics is essential to design counters which are used in building complex system in medical field like ECG counter.
CO10	PO2	L2	Simple mathematical analysis is required to build complex system like micro-controllers, timers using basic counters.
CO10	PO3	L2	Strong foundation in designing counter circuits enables to provide design solutions for complex engineering problems like timers and counters in processors and controllers.
CO11	PO1	L1	Basic knowledge of mathematics is essential to design adder and subtractors which are used in building complex system like Digital signal processors and ASIC's.
CO11	PO2	L2	Simple mathematical analysis is required to build complex system like DSP Processors using basic adder and subtractors.
CO11	PO3	L2	Strong foundation in designing adder and subtractor circuits enables to provide design solutions for complex engineering problems like ASIC's and high speed processors.
CO11	PO5	L2	Modern tool Multisim is used for designing the adder and subtractor circuits which can be used to model complex circuits used in building complex system like ASIC's and high speed processors.
CO12	PO1	L1	Basic knowledge of mathematics is essential to design counters which are used in building complex system in medical field like ECG counter.
CO12	PO2	L2	Simple mathematical analysis is required to build complex system like micro-controllers, timers using basic counters.
CO12	PO3	L2	Strong foundation in designing counter circuits enables to provide design solutions for complex engineering problems like timers and counters in processors and controllers.
CO12	PO5	L2	Modern tool Multisim is used for designing the counter circuits which can be used to model complex circuits used in building complex system like ASIC's and high speed processors.

Note: Write justification for each CO-PO mapping.

5. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					

Note: Write Gap topics from A.4 and add others also.

6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					

Note: Anything not covered above is included here.

C. COURSE ASSESSMENT

1. Course Coverage

Unit	Title	Teaching Hours	No. of question in Exam							CO	Levels
			CIA-1	CIA-2	CIA-3	Asg-1	Asg-2	Asg-3	SEE		
1	De-Morgan's law &Boolean expression relization using logic gates	03	1	–	–	–	–	–	1	CO1	
2	FullAdderandSubtractor	03	1	–	–	–	–	–	1	CO2	
3	Parallel Adder/Subtractor using 7483	03	1	–	–	–	–	–	1	CO3	
4	Comparators	03	1	–	–	–	–	–	1	CO4	
5	Multiplexer	03	1	–	–	–	–	–	1	CO5	
6	Demultiplexerand Decoder	03	1	–	–	–	–	–	1	CO6	
7	Study of Flip-Flops	03	–	1	–	–	–	–	1	CO7	
8	ShiftRegisters	03	–	1	–	–	–	–	1	CO8	
9	RingCounter andJohnsonCounter	03	–	1	–	–	–	–	1	CO9	
10	Counters	03	–	–	1	–	–	–	1	CO10	
11	Simulate Serial- Adder using simulation tool.	03	–	–	1	–	–	–	1	CO11	

12	Simulate Binary Multiplier using simulation tool.	03	–	–	1	–	–	–	1	CO12	
-	**Total**	**36**	**6**	**3**	**3**				**12**	-	-

Note: Write CO based on the theory course.

2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	CO	Levels
CIA Exam – 1	30	CO1, CO2, CO3, CO4	L23, L3
CIA Exam – 2	30	CO5, CO6, CO7,	L1, L2, L3 . .
CIA Exam – 3	30	CO8, CO9	L1, L2, L3 . .
Assignment - 1	05	CO1, CO2, CO3, CO4	L2, L3, L4 …
Assignment - 2	05	CO5, CO6, CO7, CO8, CO9	L1, L2, L3 …
Assignment - 3	05	CO8, CO9	L1, L2, L3 …
Seminar - 1	05	CO1, CO2, CO3, CO4	L2, L3, L4 . ..
Seminar - 2	05	CO5, CO6,CO7,CO8, CO9	L2, L3, L4 . ..
Seminar - 3	05	CO8, CO9	L2, L3, L4 . ..
Other Activities – define –Slip test		CO1 to Co9	L2, L3, L4 . ..
Final CIA Marks	**40**	-	-

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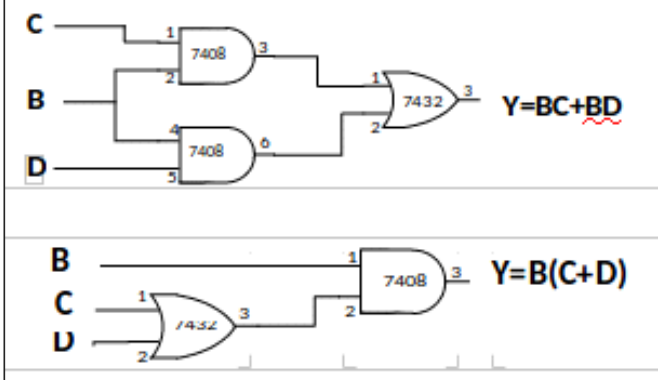
SNo	Description	Marks
1	Observation and Weekly Laboratory Activities	05 Marks
2	Record Writing	10 Marks for each Expt
3	Internal Exam Assessment	25 Marks
4	Internal Assessment	40 Marks
5	SEE	60Marks
-	**Total**	**100 Marks**

D. EXPERIMENTS

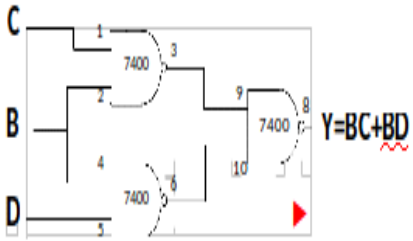
Experiment 01 : De-Morgan's law & Boolean expression relization using logic gates

-	**Experiment No.:**	1	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	De-Morgan's law &Boolean expression relization using logic						

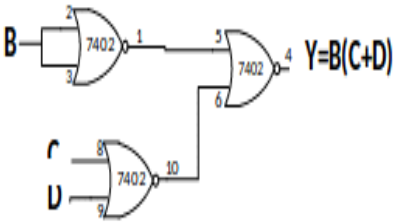
		gates
2	Course Outcomes	Verify &understand De-Morgan's theorem &realize the boolean expression using logic gates
3	Aim	To verify a) De-Morgan's theorem for 2-variables b) The Sum-of-Product and Product-of-sum expression using universal gates
4	Material / Equipment Required	Lab Manual IC 7408 (AND), IC 7404 (NOT), IC 7432 (OR),IC 7400 (NAND), IC7402 (NOR),IC 7486 (EX-OR)
5	Theory, Formula, Principle, Concept	**Given Problem:** $Y = f\ A,B,C,D = \overline{A}B\overline{C}D + \overline{A}BC\overline{D} + \overline{A}BCD + AB\overline{C}D + ABC\overline{D} + ABCD$
6	Procedure	1.Verify that the gates areworking. 2.Constructa truth table for the given problem. 3.Draw a Karnaugh Mapcorresponding to the given truth table. 4.Simplify the given Boolean expressionmanuallyusing the Karnaugh Map. **A:ImplementationUsing Logic Gates** 5.Realizethe simplified expression using logic gates. 6.Connect V_{cc}andground as shown in the pin diagram. 7.Make connections as per the logic gate diagram. 8.Apply the different combinations of input according to the truth tables. 9.Check the output readings for the given circuits;check themagainst the truth tables.

		10.Verify that the results are correct. **B.ImplementationUsing UniversalGates** 11.Convertthe AND-OR logic intoNAND-NANDand NOR-NOR logic. 12.Implement the simplified Boolean expressions using only NAND gates, and then using only NORgates. 13.Connect the circuits according to the circuit diagrams, apply inputs accordingto thetruth table and verify the results.
7	Block, Circuit, Model Diagram, Reaction\ Equation, Expected Graph	**Expression Realization using Basic Gates:** 

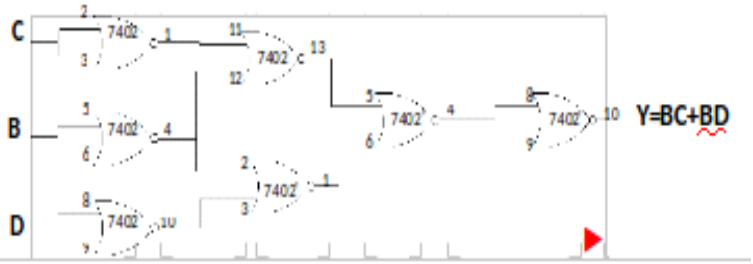
Realization using only NAND gates:



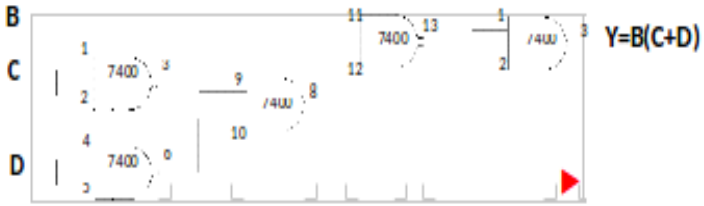
Realization using only NOR gates:



Realization using only NOR gates:



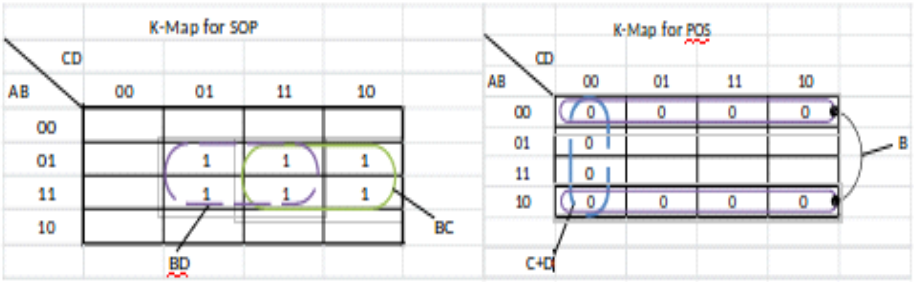
Realization using only NAND gates:



8	TruthTable, Output	

Truth Table:

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

9	Sample Calculations	**Switching Expression:** $\sum m(5,6,7,13,14,15)$ π **KarnaughMapSimplification:**  **Simplified Boolean Expression:** SOP form $Y=f(A,B,C,D)=BC+BD$ POS form $Y=f(A,B,C,D)=B(C+D)$
10	Results &Analysis	Compare with truth table

11	Application Areas	Engineering – Building circuits,Set Theory – Venn diagrams, Java
12	Remarks	
13	Faculty Signature with Date	

Experiment 02 : Full Adder and Subtractor

-	**Experiment No.:**	2	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	FullAdderandSubtractor						
2	Course Outcomes	Analyze the full adder/subtractor logic using logic gates						
3	Aim	To realize half/fulladder and half/fullsubtractorusing Logic gates						
4	Material / Equipment Required	Lab Manual IC 7408, IC 7432, IC 7486, IC 7404, etc.						
5	Theory, Formula, Principle, Concept	Full adder: $S = A \oplus B \oplus C_{n-1}$ $C = (A \oplus B) C_{n-1} + AB$ Full subtractor: $D = A \oplus B \oplus C_{n-1}$ $\bar{A}B + C_{n-1}(\overline{A \oplus B})$						

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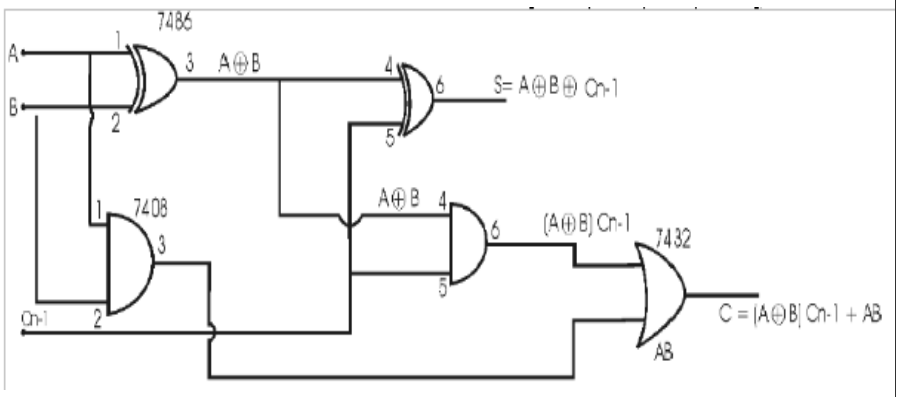
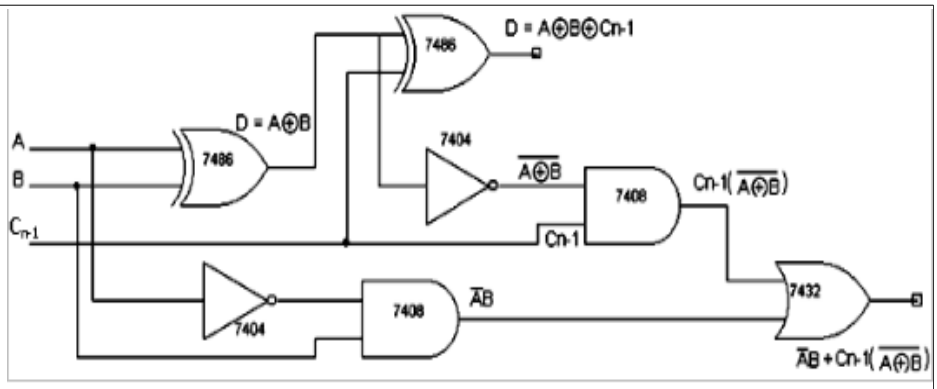
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1.Verify that the gates areworking. 2.Make theconnections as per the circuitdiagramfor the fulladder circuit, on thetrainer kit. 3.SwitchontheVCCpowersupplyandapplythevariouscombinationso ftheinputs according tothe respective truth tables. 4.Note down the output readings for the full adder circuit for the corresponding combination ofinputs. 5.Verify that the outputs are accordingto the expected results. 6.Repeattheprocedureforfullsubtractor circuit. 7.Verifythatthesum/differenceandcarry/borrowbitsareaccordingtothee xpected values.
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	**Full Adder Using Logic Gates** 



Full Subtractor Using Logic Gates

8 TruthTable

Full Adder Using Basic Gates

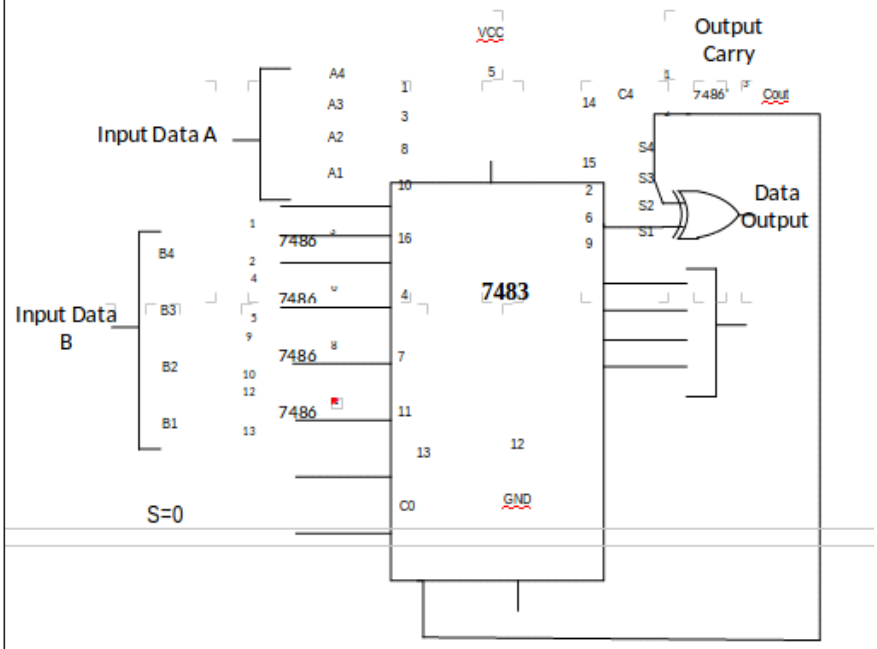
A	B	C_{n-1}	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

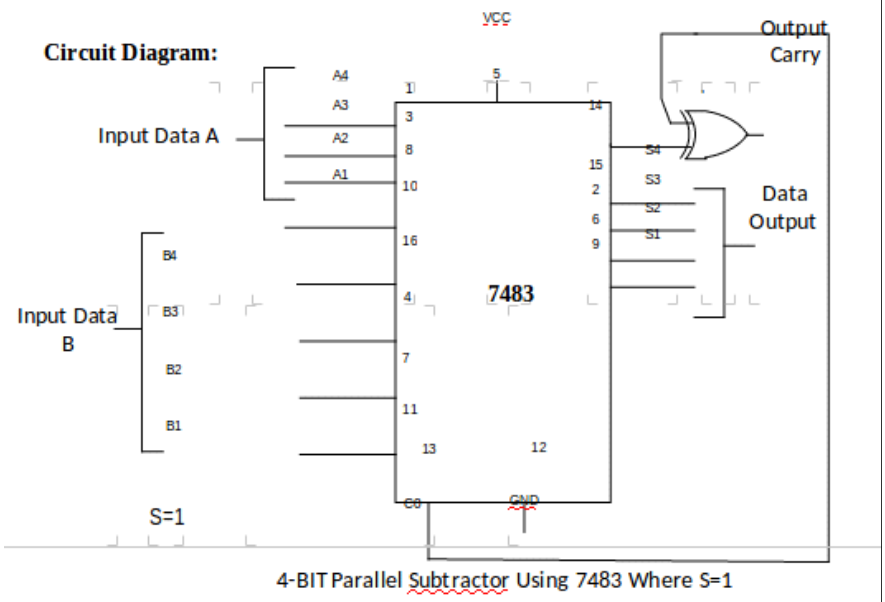
Full Subtractor Using Basic Gates				
A	B	C_{n-1}	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

9	Sample Calculations	-
10	Results &Analysis	Compare the output in the trainer kit with truth table
11	Application Areas	Integrated in the calculators and At Networking side the Full adder is used mostly.
12	Remarks	
13	Faculty Signature with Date	

Experiment 03 : PARALLEL ADDER AND SUBTRACTOR USING 7483

-	**Experiment No.:**	3	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	PARALLELADDER ANDSUBTRACTOR USING7483						
2	Course Outcomes	Design the parallel adder &subtractor circuits and compare both the circuits						
3	Aim	TorealizeParallel Adder and Subtractor Circuits using IC 7483						
4	Material / Equipment Required	Lab Manual IC 7483, IC 7486, etc.						
5	Theory, Formula, Principle, Concept							
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1.ConnectonesetofinputsfromA1toA4pinsandtheothersetfromB1toB4,on the IC 7483. 2.Connectthepins fromS1 to S4 to output terminals. 3.ShortS,C0toXORgate1inputandotherinputtakefromC4 andobtainthe OutputCarry Cout (Output Borrow Bout). 4.In ordertoPerform Addition take S=0. 5.InordertoimplementtheIC7483asasubtractor,TakeS=1,ApplytheBinput throughXOR gates (essentially taking complement ofB). 6.Apply the inputs to theadder/ subtractorcircuits as shown in the truth						

		tables. 7.Check the outputs and note themdown in the table for the corresponding inputs. 8.Verify that the outputsmatch with the expectedresults.
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• **A.IC 7483 as a ParallelAdder** **CircuitDiagram:**  4-BIT Parallel Adder Using 7483 where S=0 **uth Table:**

		B.IC 7483 as a Parallel Subtractor **Circuit Diagram:**  4-BIT Parallel Subtractor Using 7483 Where S=1
8	Observation Table, Look-up Table, Output	

A.IC 7483 as a ParallelAdder

Truth Table:-

Input Data A				Input Data B				Addition				
A4	A3	A2	A1	B4	B3	B2	B1	Cout	S4	S3	S2	S1
1	0	0	0	0	0	1	0	0	1	0	1	0
1	0	0	0	1	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	1	0	1	0
0	0	0	1	0	1	1	1	0	1	0	0	0
1	0	1	0	1	0	1	1	1	0	1	0	1
0	1	1	0	0	0	1	1	0	1	0	0	1
1	1	1	0	1	1	1	1	1	1	1	0	1
1	0	1	0	1	1	0	1	1	0	1	1	

B.IC 7483 as a Parallel Subtractor

Truth Table:

Input Data A				Input Data B				Subtraction				
A4	A3	A2	A1	B4	B3	B2	B1	Bout	S4	S3	S2	S1
1	0	0	0	0	0	1	0	0	0	1	1	0
1	0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	1	1	0	1	0
0	0	0	1	0	1	1	1	1	1	0	1	0
1	0	1	0	1	0	1	1	1	1	1	1	1
0	1	1	0	0	0	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	0	1	1	1	1	0	1

Note: Bout = 1 for A<B; Bout = 0 for A>B;

9	Sample Calculations	**Example**

4bita ddero perati onusi ng 7483

ifcontrolinput S=0,additioncan beperformed

Ex:If

↓C0=0

$A_4 A_3 A_2 A_1$=1100

$B_4 B_3 B_2 B_1$=0011

thenSum,$S_4 S_3 S_2 S_1$ =1111

andC0 C4= Cout.

- **4bit subtraction operation using 7483 forA>Bhere S=1**

$A_4 A_3 A_2 A_1$ =

1001

B_4 B_3 B_2 B_1 =

1101 (2's complement) of+3=0011

The end around carry is disregarded 1 0110

C0⊕C4 = Bout = 0

Difference, $S_4 S_3 S_2 S_1$ = 0110

2's complement method of subtraction can be performed, if S=1(i.e. C0=1).

Consider the above Example $A_4 A_3 A_2 A_1$= 1001 and $B_4 B_3 B_2 B_1$= 0011

1"s Complement of $B_4 B_3 B_2 B_1$ is $\overline{B_4}\,\overline{B_3}\,\overline{B_2}\,\overline{B_1}$= 1100

$A_4 A_3 A_2 A_1$ = 1001

$B_4 B_3 B_2 B_1$ = 1100 → (1's complement) of +3 = 0011 } 2"s Complement of B input = -B

+1 ← C0=1(S&C0 shorted)

The end around carry is disregarded (1)0110

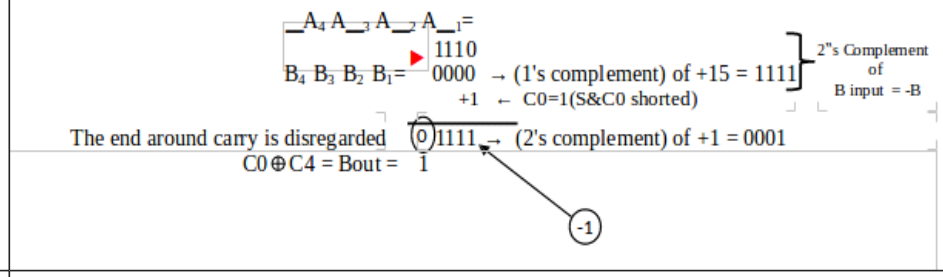
C0⊕C4 = Bout = 0 +6

- **4 bit subtraction operation using 7483 for A<B here S=1**

EC

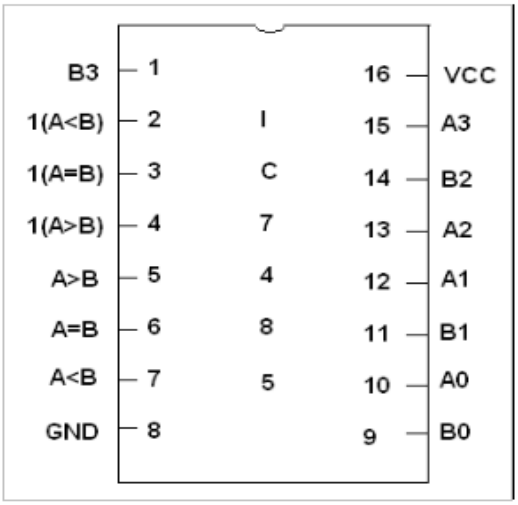
Prepared by Checked by

Approved

		
10	Results &Analysis	Do the calculations and compare with truthtable
11	Application Areas	CPLD applications and VHDL circuits and devices
12	Remarks	
13	Faculty Signature with Date	

Experiment 04 : Comparator

-	**Experiment No.:**	4	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Comparator						
2	Course Outcomes	Evaluate the performance of 4-bit magnitude comparator using 7485 IC						
3	Aim	To realize 4 bit magnitude comparator using IC 7485						
4	Material / Equipment Required	IC 7485						
5	Theory, Formula, Principle, Concept							
6	Procedure, Program, Activity, Algorithm, Pseudo Code	**1.**Verify the workingofthe logic gates. **2.**Make theconnections as per therespective circuit diagrams. **3.**Switch on Vcc. **4.**Apply the inputs as per the truth tables. **5.**Write the truth table for an 5-bit comparator.						

		6.Connect pin16 to V_{cc}andpin 8 to GNDfor the ICs. **7.**Apply the two inputs asshown; making surethatthe MSB and LSBis correctly connected. **8.**Outputs arerecorded at pin 2 (A<B), pin 4 (A>B), pin 3 (A=B) pins andare verified as being according to thetruth table.
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	**5-Bit comparator using IC 7485** **PinDiagram:** 

8	Truth Table, Output	**Truth Table: 4bit Comparator**

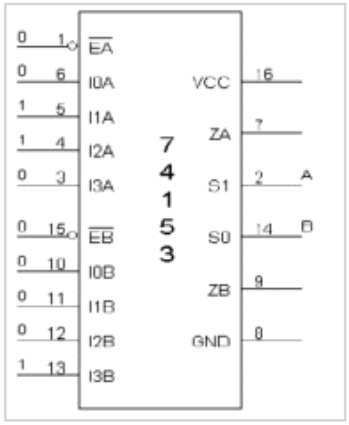
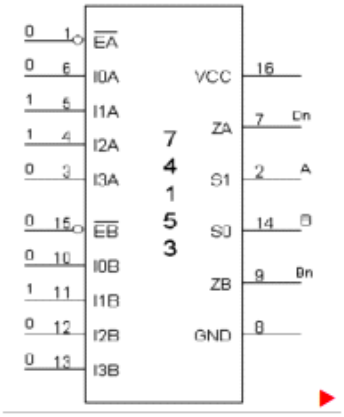
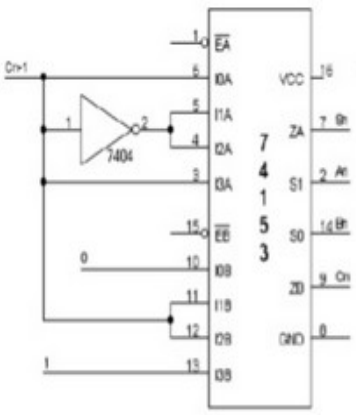
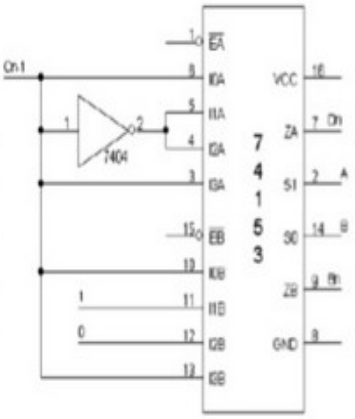
Input A				Input B				Output		
A3	A2	A1	A0	B3	B2	B1	B0	A>B	A<B	A=B
0	0	0	0	0	0	0	1	0	1	0
0	1	0	1	0	0	1	1	1	0	0
1	0	1	0	1	0	1	0	0	0	1
0	0	1	1	0	1	1	0	0	1	0
0	1	0	0	1	0	0	0	0	1	0
1	1	0	1	1	0	1	1	1	0	0
0	1	1	0	0	1	1	0	0	0	1
1	1	1	1	1	1	1	0	1	0	0

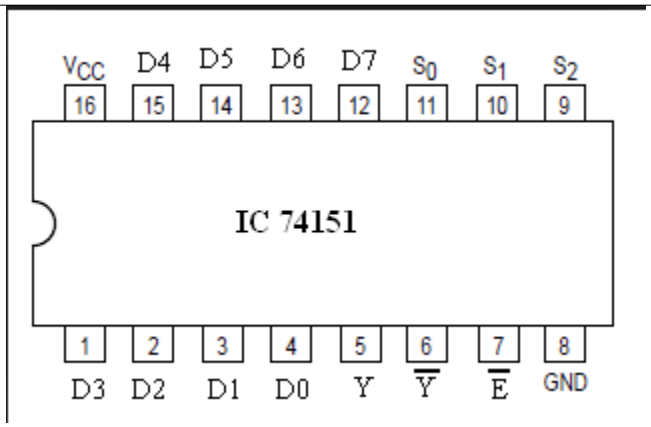
9	Sample Calculations	
10	Results &Analysis	Compare the output with trainer kit
11	Application Areas	Generally, in electronics, the comparatoris used to compare two voltages or currents
12	Remarks	
13	Faculty Signature with Date	

Experiment 05 : Multiplexer

-	**Experiment No.:**	5	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Multiplexer						
2	Course Outcomes	Realize 4:1 mux &8:1 mux and Analyze the both						
3	Aim	To realize - Adder &Subtractor using IC 74153 - 3 variable function using IC 74151 (8:1 mux)						
4	Material / Equipment Required	Lab Manual IC74151,IC 74153, IC 7400, IC 7420, IC74138,IC7404,IC7408,IC7432 etc						
5	Theory, Formula, Principle, Concept	For mux using Ic 74151						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	**A.For MUXIC 74153** **1.**The Pin [16] isconnectedto + Vcc andPin[8]is connectedto ground. **2.**The inputsare appliedeither to 'A'input or 'B' input. **3.**IfMUX'A'hastobeinitialized,E_A ismadelowandifMUX'B'hastobe initialized,$E_B$ismadelow. **4.**Basedontheselectionlinesoneoftheinputswillbeselectedatth						

		e output,and thus thetruth tableisverified. **5.**IncaseofhalfadderusingMUX,applyconstantinputsat(I_{0a},I_{1a},I_{2a}, I_{3a})and(I_{0b},I_{1b},I_{2b}andI_{3b})as shown. **6.**Thecorrespondingvaluesofselectinputlines,AandB(S_1 andS_0)are changedaspertableandtheoutputistakenatZ_a assumandZ_b as carry. **7.**Inthiscase,theinputsAandBarevaried.MakingE_a andE_b zero andthe outputis taken at Z_a,and Z_b. **8.**IncaseofHalfSubtractor,connectionsaremadeaccordingtothe circuit, InputsareappliedatAandBasshown,andoutputsaretakenat Z_a(Difference)and Z_b(Borrow). Verify outputs. **9.**InfulladderusingMUX,theinputsareappliedatC_{n-1},A_n andB_n accordingtothetruthtable.Thecorrespondingoutputsaretakena tS_n (pinZ_a)and C_n(pinZ_b)and are verifiedaccording to thetruth table. **10.**InfullsubtractorusingMUX,theinputsareappliedatC_{n-1},A_n and$B_n$according tothetruthtable.Thecorrespondingoutputsaretakenat pinZ_a(Difference)andpinZ_b(Borrow)andareverifiedaccordin gtothe truthtable.

7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	**Half AdderUsing 74153** **Half Subtractor using 74153**   **Full Adder Using 74153** **Full Subtractor using 74153**   **3. 8:1 Mux using IC 74151**



8 Observation Table, Look-up Table, OutputRefer Lab manual

Truth Table:

Inputs		Half Adder Outputs		Half Subtractor Outputs	
A	B	Sum	Carry	Diff	Borrow
0	0	0	0	0	0
0	1	1	0	1	1
1	0	1	0	1	0
1	1	0	1	0	0

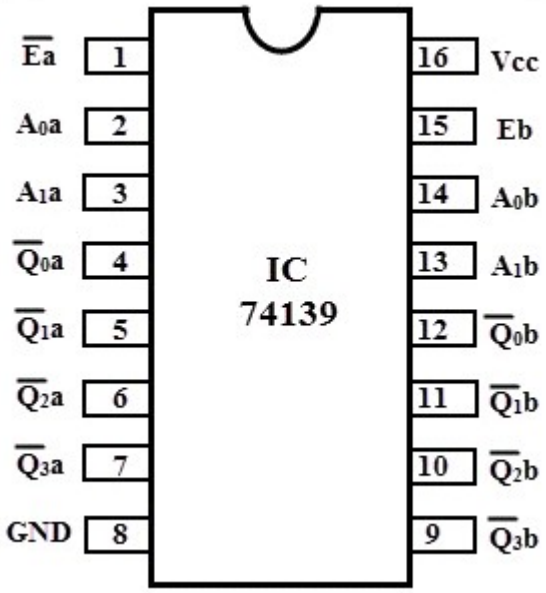
Truth Tables for Full Adder/Subtractor using 74153

Inputs			Full Adder Outputs		Full Subtractor Outputs	
A	B	C_{in}/B_{in}	S	C_{out}	D	B_{out}
0	0	0	0	0	0	0
0	0	1	1	0	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	1	0	0	1	0	0
1	1	1	1	1	1	1

9	Sample Calculations	
10	Results &Analysis	compare with truth tables
11	Application Areas	• Communication System for the process of data transmission.
12	Remarks	
13	Faculty Signature with Date	

Experiment 06 : Decoder

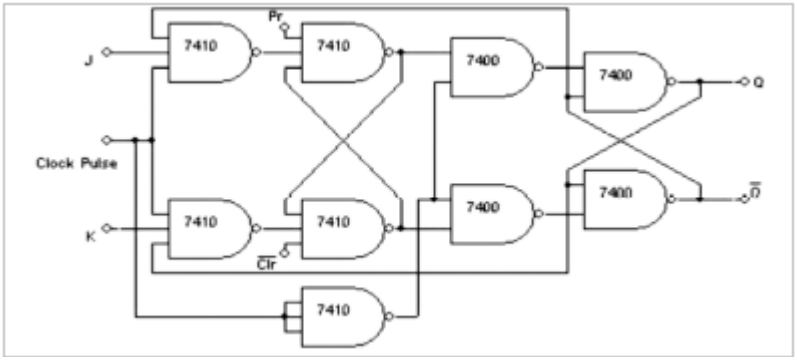
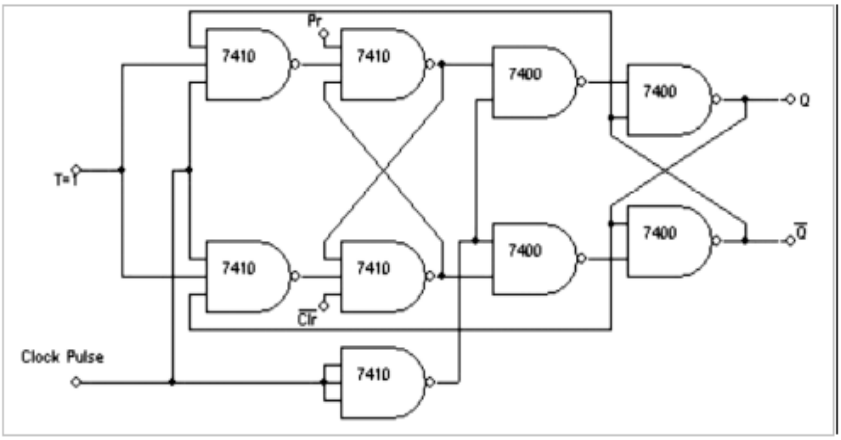
-	**Experiment No.:**	6	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	De-multiplexer &Decoder						
2	Course Outcomes	Realize Decoder using 74139IC						
3	Aim	To realize decoder using IC 74139						
4	Material / Equipment Required	IC 74139						
5	Theory, Formula, Principle, Concept							
6	Procedure, Program, Activity, Algorithm, Pseudo Code	**1.**Verify the workingofthe logic gates. **2.**Make theconnections as per therespective circuit diagrams. **3.**Switch on Vcc. **4.**Apply the inputs as per the truth tables. **5.**Write the truth table.						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							


Ea 1
A0a 2
A1a 3
Q0a 4
Q1a 5
Q2a 6
Q3a 7
GND 8
16 Vcc
15 Eb
14 A0b
13 A1b
12 Q0b
11 Q1b
10 Q2b
9 Q3b
IC
74139

8	Observation Table, Look-up Table, Output	
9	Sample Calculations	
10	Results &Analysis	compare with truth table
11	Application Areas	• Communication System which converts multiplexed signals back to the original form/ wireless or wired media
12	Remarks	
13	Faculty Signature with Date	

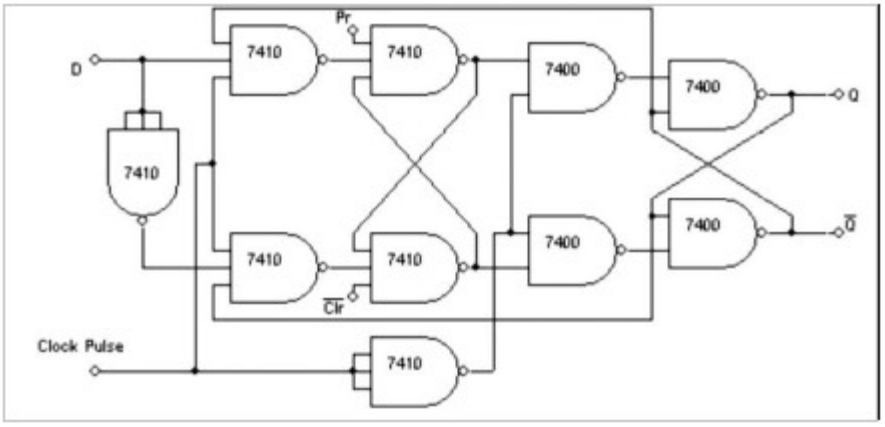
Experiment 07 : STUDY OF FLIP-FLOPS

-	**Experiment No.:**	7	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Study of flip flops						
2	Course Outcomes	Realize the operation of master slaveJK, D &T flip-flop.						
3	Aim	Tostudy and verify the truthtables for master slaveJK, D &T flip-flop.						
4	Material / Equipment Required	IC 7410, IC 7400, etc.						
5	Theory, Formula, Principle, Concept	Lab Manual						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1.Make theconnections as shown in the respectivecircuitdiagrams. 2.Apply inputs as shown in the respective truth tables, for each ofthe flip-flop circuits. 3.Checktheoutputsofthecircuits;verifythattheymatchthatoftherespectivetruth tables.						
7	Block, Circuit, Model	**A.J-K Master-Slave Flip-Flop**						

	Diagram, Reaction Equation, Expected Graph	**Circuit:**  **B. T-Type Flip-Flop** **Circuit:** 

C.D-Type Flip-Flop

Circuit:



8 Observation Table, Look-up Table, Output

A.J-K Master-Slave Flip-Flop

Truth Table :

Preset	Clear	J	K	Clock	Q_{n+1}	Q_{n+1}	Status
0	1	X	X	X	1	0	Set
1	0	X	X	X	0	1	Reset
1	1	0	0	⎍			No Change
1	1	0	1		0	1	Reset
1	1	1	0	⎍	1	0	Set
1	1	1	1	⎍			Toggle

B. T-Type Flip-Flop

Truth Table :

Preset	Clear	T	Clock	Q_{n+1}	$\overline{Q_{n+1}}$
1	1	0	⎍	Qn	$\overline{Qn}$
1	1	1	⎍	$\overline{Qn}$	Qn

C.D-Type Flip-Flop:

Truth Table:

Preset	Clear	D	Clock	Q_{n+1}	Q_{n+1}
1	1	0	↑	0	1
1	1	1	↑	1	0

9	Sample Calculations	
10	Results &Analysis	Compare with truth table • Master slave JK , D &T flip flop arerealised and verified.
11	Application Areas	• main components of sequential circuits, storing of binary data, counter, transferring binary data from one location to other
12	Remarks	
13	Faculty Signature with Date	

Experiment 08 : STUDY OF SHIFT REGISTERS

-	**Experiment No.:**	8	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Study of shift registers						
2	Course Outcomes	Understand the operation of shift registers						

3	Aim	To study IC 74S95, and the realization of SIPO, SISO, PISO, PIPO ,RingCounter andJohnsonCounteroperations usingthe same.
4	Material / Equipment Required	IC 7495, IC 7495, IC 7404, etc.
5	Theory, Formula, Principle, Concept	
6	Procedure, Program, Activity, Algorithm, Pseudo Code	**A.Serial In-Parallel Out(Left Shift):** 1. Make theconnections as shown in the respectivecircuitdiagram. 2. Makesurethe7495isoperatinginParallelmodebyensuringPin6(ModeM) issetto HIGH, and connectclock input to Pin 8 (Clk 2). 3. Applythefirstdataatpin5(D)andapplyoneclockpulse.We observethat this data appears at pin 10 (Q_D). 4. Now,applytheseconddataatD.Applyaclockpulse.Wenowobserv ethat theearlier data is shiftedfrom$Q_D$toQ_C,and the new data appears at Q_D. 5. Repeat theearlier step to enterdata,untilall bitsare enteredone by one. 6. Attheendofthe4th clockpulse,wenoticethatall4bitsareavailableatthe parralleloutput pins Q_A(MSB), Q_B,Q_C,Q_D(LSB).

		7. Entermorebitstoseethereisaleftshiftingofbitswitheach succeedingclock pulse. **B.Serial In-Parallel Out(Right Shift):** 1. Make theconnections as shown in the respectivecircuitdiagram. 2. Makesurethe7495isoperatinginSIPOmodebyensuringPin6(ModeM)is settoLOW,and connect clock inputto Pin9 (Clk 1). 3. Applythefirstdataatpin1(SD1)andapplyoneclockpulse.Weobservethat this data appears at pin 13 (Q_A). 4. Now,applytheseconddataatSD1.Applyaclockpulse.Wenowobservethat theearlier data is shiftedfrom$Q_A$toQ_B,and the new data appears at Q_A. 5. Repeat theearlier step to enterdata,untilall bitsare enteredone by one. 6. Attheendofthe4th clockpulse,wenoticethatall4bitsareavailableatthe parallel output pins $Q_A$through Q_D. 7.

Entermorebitstoseethereisarightshiftingofbitswitheachsucceeding

clockpulse.

C.Serial In-SerialOut Mode:

1. Connectionsare made as shown in the SISO circuitdiagram.

2.

Makesurethe7495isoperatinginSIPOmodebyensuringPin6(Mode)isset to LOW, and connectclock input toClk 1(Pin 9).

3.

The4bitsareappliedattheSerialInputpin(Pin1),onebyone,withaclock pulsein between each pair of inputsto loadthe bits into the IC.

4. Attheendofthe4th clockpulse,thefirstdatabit, „d0" appearsattheoutputpin

Q_D.

5. Applyanotherclockpulse,togettheseconddatabit,„d1"atQ_D.Applyingyet

anotherclock pulse getsthe third data bit „d2"atQ_D,and so on.

6.

ThusweseetheIC7495operatinginSISOmode,withseriallyappliedinputs appearing asserial outputs.

D.Parallel In-SerialOut Mode:

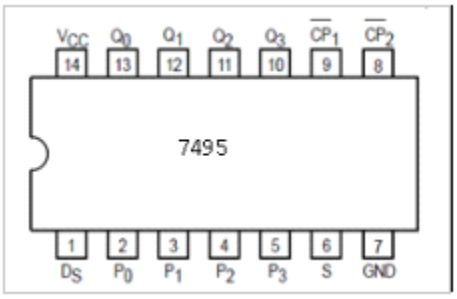
1. Connectionsare made as shown in the PISO circuitdiagram.
2. Nowapplythe4-bitdataattheparallelinputpinsA,B,C,D(pins2through 5).
3. KeepingthemodecontrolMonHIGH,applyoneclockpulse. Thedata applied attheparallelinputpinsA,B,C,Dwillappearattheparallelou tputpinsQ_A,Q_B,Q_C,$Q_D$respectively.
4. NowsettheModeControlMtoLOW,andapplyclockpulsesonebyon e.

   Observethedata coming outin a serial mode atQ_D.
5. WeobservenowthattheICoperatesinPISOmodewithpara llelinputsbeing transferred to the outputsideserially.

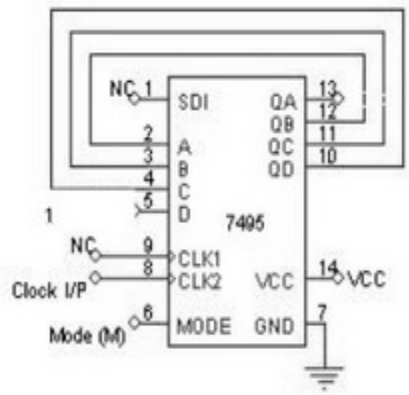
E.Parallel In-Parallel Out Mode:

1. Connectionsare made as shown in the PIPOmode circuit diagram.
2. Set Mode Control M toHIGHto enableParalleltransfer.

		3. Apply the 4data bits asinput to pinsA, B, C, D. 4. Apply one clock pulse at Clk 2 (Pin 8). 5. Notethatthe4bitdataatparallelinputsA,B,C,Dappearsatt heparallel outputpinsQ_A, Q_B,Q_C,$Q_d$respectively. Ring counter procedure: **Procedure:-** 1. Make theconnections as shown in the respectivecircuitdiagramfor the Ring Counter. 2. Apply an initial input (1000) attheA, B, C, D pins respectively. 3. Keep SelectMode = HIGH (1)and apply one clock pulse. 4. Next, SelectMode = LOW(0)to switch to serialmode and apply clock pulses. 5. Observe theoutputafter each clock pulse, recordthe observations and verify that they match the expectedoutputs from the truthtable. 6. Repeat the same procedure as abovefor the Johnson Counter circuitand verify its operation.
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	**IC7495 Pin Diagram:**



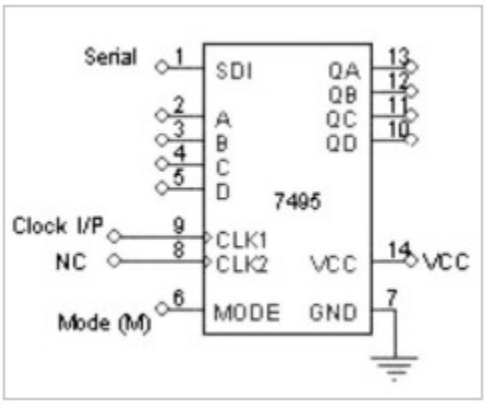
A.SIPO Mode (Left Shift)



Circuit:

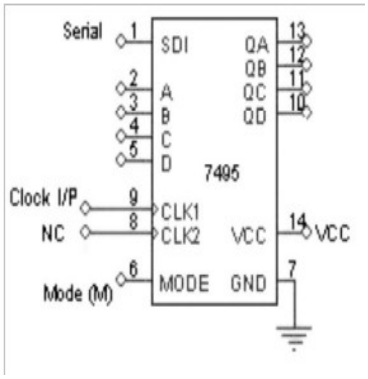
B. SIPO MODE(Right Shift)

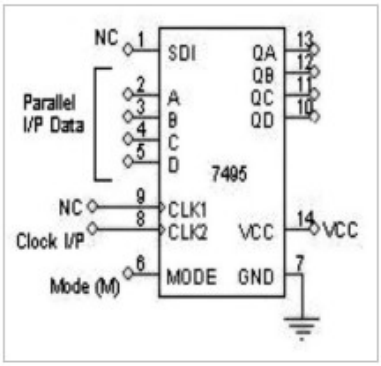
Circuit:



C.SISO Mode

Circuit:



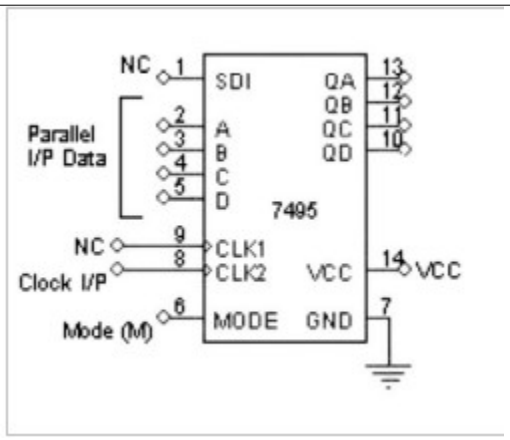


D.PISO Mode

Circuit:

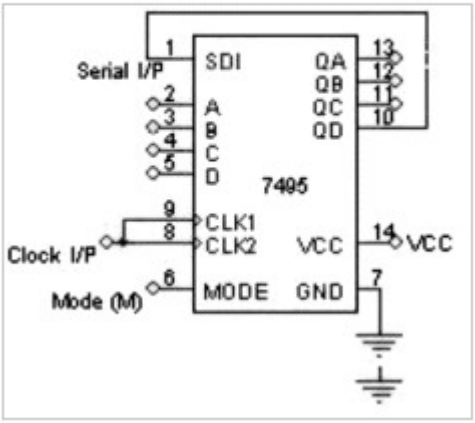
E. PIPO Mode

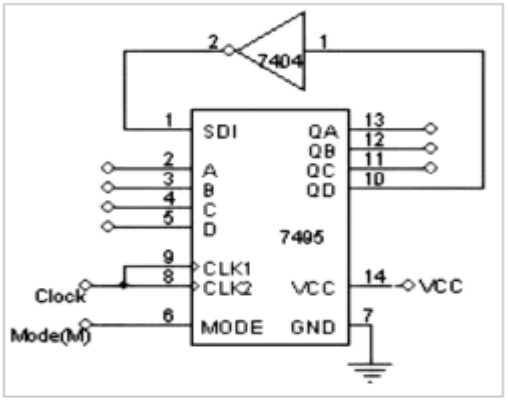
Circuit:



F.Ring Counter

Circuit:


Serial I/P
SDI
QA
QB
QC
QD
A
B
C
D
7495
CLK1
CLK2
VCC
MODE
GND
Clock I/P
Mode (M)
1
2
3
4
5
9
8
6
13
12
11
10
14
7

		Circuit:  **G.Johnson Counter**
8	Observation Table, Look-up Table, Output	**A.SIPO Mode (Left Shift)**

Truth Table:

Clock	Serial I/P	Q_A	Q_B	Q_C	Q_D
1	1	X	X	X	1
2	0	X	X	1	0
3	1	X	1	0	1
4	1	1	0	1	1

B. SIPO MODE(Right Shift)

Truth Table:

Clock	Serial I/P	Q_A	Q_B	Q_C	Q_D
1	1	1	X	X	X
2	0	0	1	X	X
3	1	1	0	1	X
4	1	1	1	0	1

C.SISO Mode

Truth table:

Clock	Serial I/P	Q_A	Q_B	Q_C	Q_D
1	**d0=0**	0	X	X	**X**
2	**d1=1**	1	0	X	**X**
3	**d2=1**	1	1	0	**X**
4	**d3=1**	1	1	1	***0=d0***
5	**X**	X	1	1	***1=d1***
6	**X**	X	X	1	***1=d2***
7	**X**	X	X	X	***1=d3***

Truth Table:

Mode	Clk	Parallel I/P				Parallel O/P			
		A	B	C	D	Q_A	Q_B	Q_C	Q_D
1	1	1	0	1	1	1	0	1	*1*
0	2	X	X	X	X	X	1	0	*1*
0	3	X	X	X	X	X	X	1	*0*
0	4	X	X	X	X	X	X	X	*1*

D.PISO Mode

E. PIPO Mode

Clk	Parallel I/P				Parallel O/P			
	A	B	C	D	Q_A	Q_B	Q_C	Q_D
1	1	0	1	1	1	0	1	1

F. Ring Counter

Truth Table:

Mode	Clock	Q_A	Q_B	Q_C	Q_D
1	1	1	0	0	0
0	2	0	1	0	0
0	3	0	0	1	0
0	4	0	0	0	1
0	5	1	0	0	0
0	6	0	1	0	0

Truth Table:

Mode	Clock	Q_A	Q_B	Q_C	Q_D
1	1	1	0	0	0
0	2	1	1	0	0
0	3	1	1	1	0
0	4	1	1	1	1
0	5	0	1	1	1
0	6	0	0	1	1
0	7	0	0	0	1
0	8	0	0	0	0
0	9	1	0	0	0
0	10	1	1	0	0

G. Johnson Counter

9	Sample Calculations	
10	Results &Analysis	Shift registers, Johnson &ring counter are realised and verified using IC 7495
11	Application Areas	• Temporary data storage, Data transfer, Data manipulation And incounters.

12	Remarks	
13	Faculty Signature with Date	

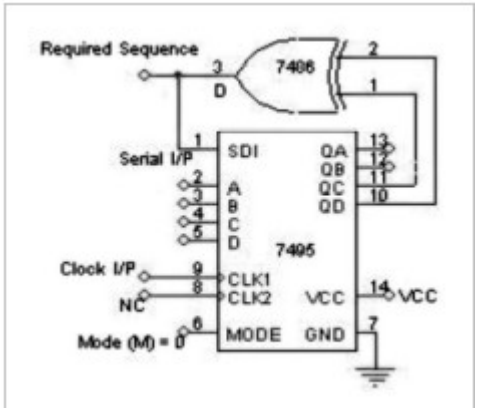
Experiment 09 : Counters

-	**Experiment No.:**	9	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Mod-N asynchronous &synchronous counters						
2	Course Outcomes	differentiate Mod-N asynchronous &synchronous counters using IC 7490 &IC 74192						
3	Aim	To design and study the operation ofMod-N asynchronous &synchronous counters.						
4	Material / Equipment Required	Lab Manual IC 7495, IC 7404, etc.						
5	Theory, Formula, Principle, Concept	Lab Manual						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• 1. Make theconnections as shown in the respectivecircuitdiagramfor the Ring • • Counter. • • 2. Apply an initial input (1000) attheA, B, C, D pins respectively. • • 3. Keep SelectMode = HIGH (1)and apply one clock pulse. • • 4. Next, SelectMode = LOW(0)to switch to serialmode and apply clock pulses. • • 5. Observe theoutputafter each clock pulse, recordthe observations and verify that they match the expectedoutputs from the truthtable. • 6. Repeat the same procedure as abovefor the Johnson Counter circuitand verify its operation.						

7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	• Lab Manual
8	Observation Table, Look-up Table, Output	• Lab Manual
9	Sample Calculations	• Lab Manual
10	Results &Analysis	• - • -
11	Application Areas	• count the data in a continuous loop, used in frequency divider circuits, 3 phase square wave generator , BCD counter etc
12	Remarks	
13	Faculty Signature with Date	

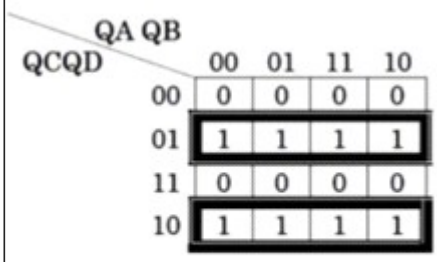
Experiment 10 : Sequence Generator

-	**Experiment No.:**	10	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Sequence Generator						
2	Course Outcomes	Realize the sequence generator and verify with truth table						
3	Aim	To design and study theoperation ofa Sequence Generator.						
4	Material / Equipment Required	IC 7495, IC 7486, etc.						
5	Theory, Formula, Principle, Concept	Inorderto generate a sequence of length „S", it is necessary to use*at least*„N"number of Flip-flops,inorder tosatisfy the condition . Thegiven sequence length S = 15 Therefore,N = 4						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1.Truth table is constructed for the given sequence,and Karnaugh maps aredrawn in order to obtain a simplified Booleanexpression for the circuit. 2.Connectionsare made as shown in the circuit diagram. 3.Mode M is set to LOW(0), and clock pulses arefed through Clk 1 (pin 9).						

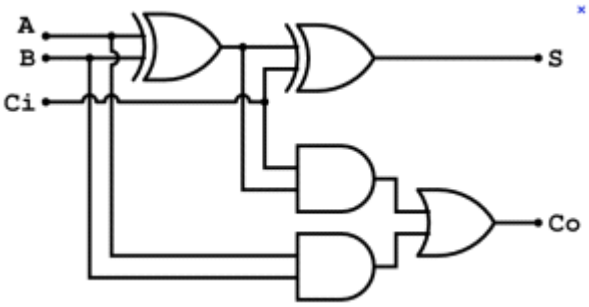
		4.Clock pulses are applied at CLK1 and the output values arenoted, and checked against the expected values fromthe truth table. 5.The functioning of the circuit asa sequence generator is verified.
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	
8	Observation Table, Look-up Table, Output	**TruthTable:**

Truth Table:

Map Value	Clock	Q_A	Q_B	Q_C	Q_D	O/p D
15	1	1	1	1	1	0
7	2	0	1	1	1	0
3	3	0	0	1	1	0
1	4	0	0	0	1	1
8	5	1	0	0	0	0
4	6	0	1	0	0	0
2	7	0	0	1	0	1
9	8	1	0	0	1	1
12	9	1	1	0	0	0
6	10	0	1	1	0	1
11	11	1	0	1	1	0
5	12	0	1	0	1	1
10	13	1	0	1	0	1
13	14	1	1	0	1	1
14	15	1	1	1	0	1
			1	1	1	
				1	1	
					1	

9	Sample Calculations	**Karnaugh Map:**  $D = \overline{Q_C} Q_D + Q_C \overline{Q_D}$
10	Results &Analysis	sequence generator is realized and truth table is verified
11	Application Areas	• Alarm clock, Set an AC timer, Set a timer for taking picture, finite state machines etc
12	Remarks	
13	Faculty Signature with Date	

Experiment 11 : Simulate Full- Adder using simulation tool.

-	**Experiment No.:**	11	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Simulate Full- Adder using simulation tool.						
2	Course Outcomes	Analyze the full adder simulation process						
3	Aim	Full adder simulation using multisim software						
4	Material / Equipment Required	Software and simulation tool						
5	Theory, Formula, Principle, Concept							
6	Procedure, Program, Activity, Algorithm, Pseudo Code	• Go to start-all • click on national instruments – circuit design suit 11.0 – multisim 11.0 • click on evaluate • click on place, go to componets • click on groups – select TTL – select requires IC • click on place – select wires • Make the connections • Click on groups – indicators – probes • click o source – digital source – interactive digital constant						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							

8	Observation Table, Look-up Table, Output	Truth table:

inputs			Output	
A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

9	Sample Calculations	
10	Results &Analysis	Full adder have been simulated &verified according to truth table
11	Application Areas	• Engineering – Building circuits,Set Theory – Venn diagrams
12	Remarks	
13	Faculty Signature with Date	

Experiment 12 : MOD-8 synchronous up/down Counter

-	**Experiment No.:**	12	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	MOD 8 synchronous up/down Counter						
2	Course Outcomes	Distinguish between MOD-8 up &downcounter operation						
3	Aim	To realize the Mod -8 synchronous up/downcounter circuit for different input combinations						
4	Material / Equipment Required	IC 74193						
5	Theory, Formula, Principle, Concept							

<table>
<tr><td>6</td><td>Procedure, Program, Activity, Algorithm, Pseudo Code</td><td>• Click on start - all programs – national instrument – circuit design – multisim 11.0-evaluate
• Click on place – group- TTL- 74LS193D
• PLACE – INDICATOR – HEX DISPLAY – DCD HEX
• Go to place – indicator- probes – select -three probes
• place – source- signal voltage source – clock voltage
• place – basics – switch SPOT
• Place – sources -power sources -Vcc
• Place – sources – power sources – DGND
• place – components- wire -make the connections as in diagram</td></tr>
<tr><td>7</td><td>Block, Circuit, Model Diagram, Reaction Equation, Expected Graph</td><td></td></tr>
<tr><td>8</td><td>Observation Table, Look-up Table, Output</td><td>
<table>
<tr><th colspan="4">COUNT-UP Mode</th><th colspan="4">COUNT-DOWN Mode</th></tr>
<tr><th>States</th><th>Q_C</th><th>Q_B</th><th>Q_A</th><th>States</th><th>Q_C</th><th>Q_B</th><th>Q_A</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>7</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>6</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>2</td><td>0</td><td>1</td><td>0</td><td>5</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>3</td><td>0</td><td>1</td><td>1</td><td>4</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>4</td><td>1</td><td>0</td><td>0</td><td>3</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>5</td><td>1</td><td>0</td><td>1</td><td>2</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>6</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>7</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>9</td><td>Sample Calculations</td><td></td></tr>
<tr><td>10</td><td>Results &Analysis</td><td>Mod -8 synchronous up/downcounter has been simulated and verified</td></tr>
<tr><td>11</td><td>Application Areas</td><td>• dividers for clock signals,finite state machines etc</td></tr>
<tr><td>12</td><td>Remarks</td><td></td></tr>
</table>

13	Faculty Signature with Date	